ABSTRACT OF THE DISCLOSURE

The DRAM drives a bit line pair connected to a read column select gate and a write column select line connected to a write column select gate by a power supply voltage for an array, and drives a read column select line connected to a read column select gate and write data line pair connected to a write column select gate by a power supply voltage for a peripheral circuitry. Hence, even when one power supply voltage becomes high and another power supply voltage becomes low at the same time, the timing margin and operation margin can sufficiently be secured. Thus, a semiconductor memory device allowing a stable high-speed operation with large timing margin and operation margin will be achieved.